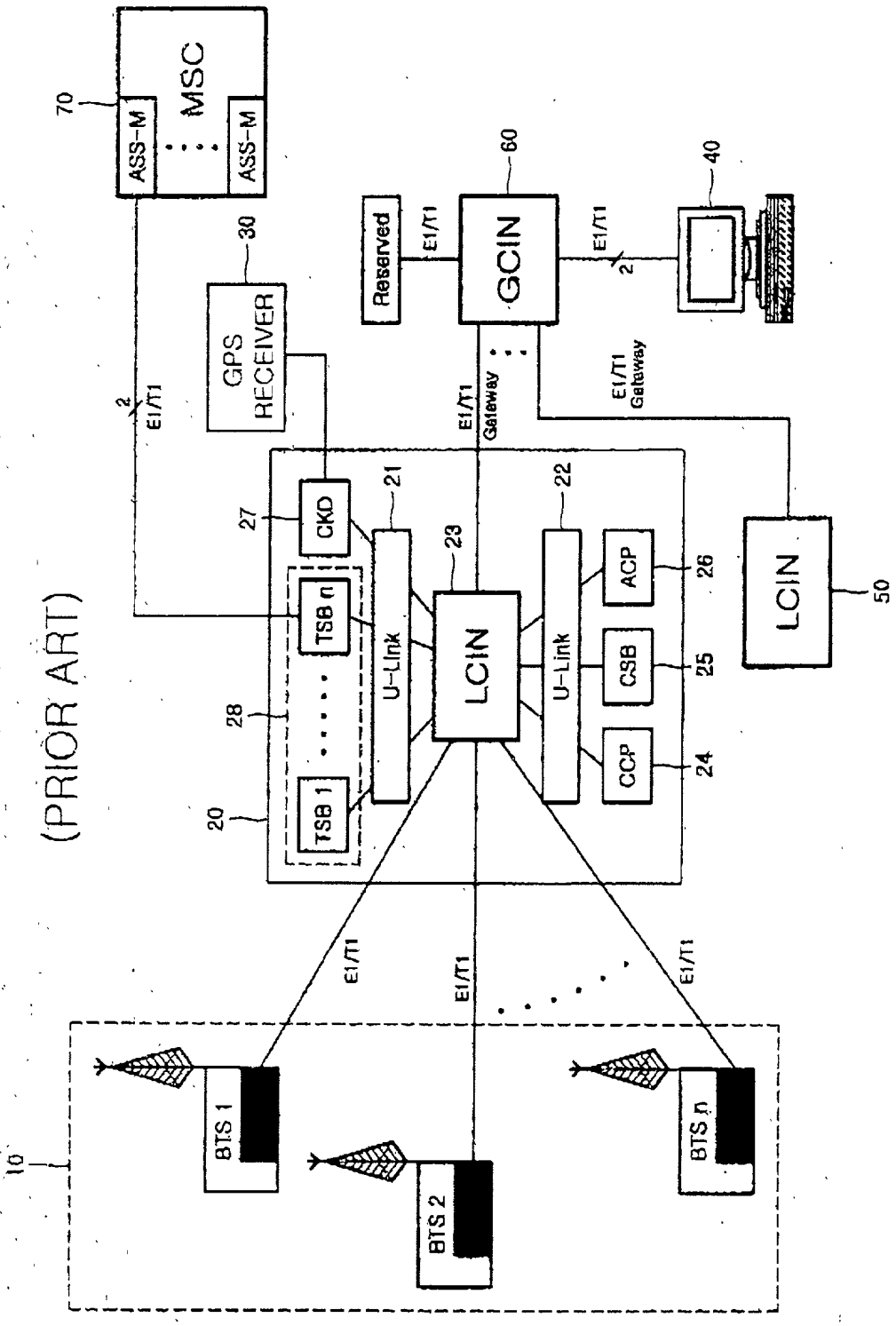


FIG. 1
(PRIOR ART)

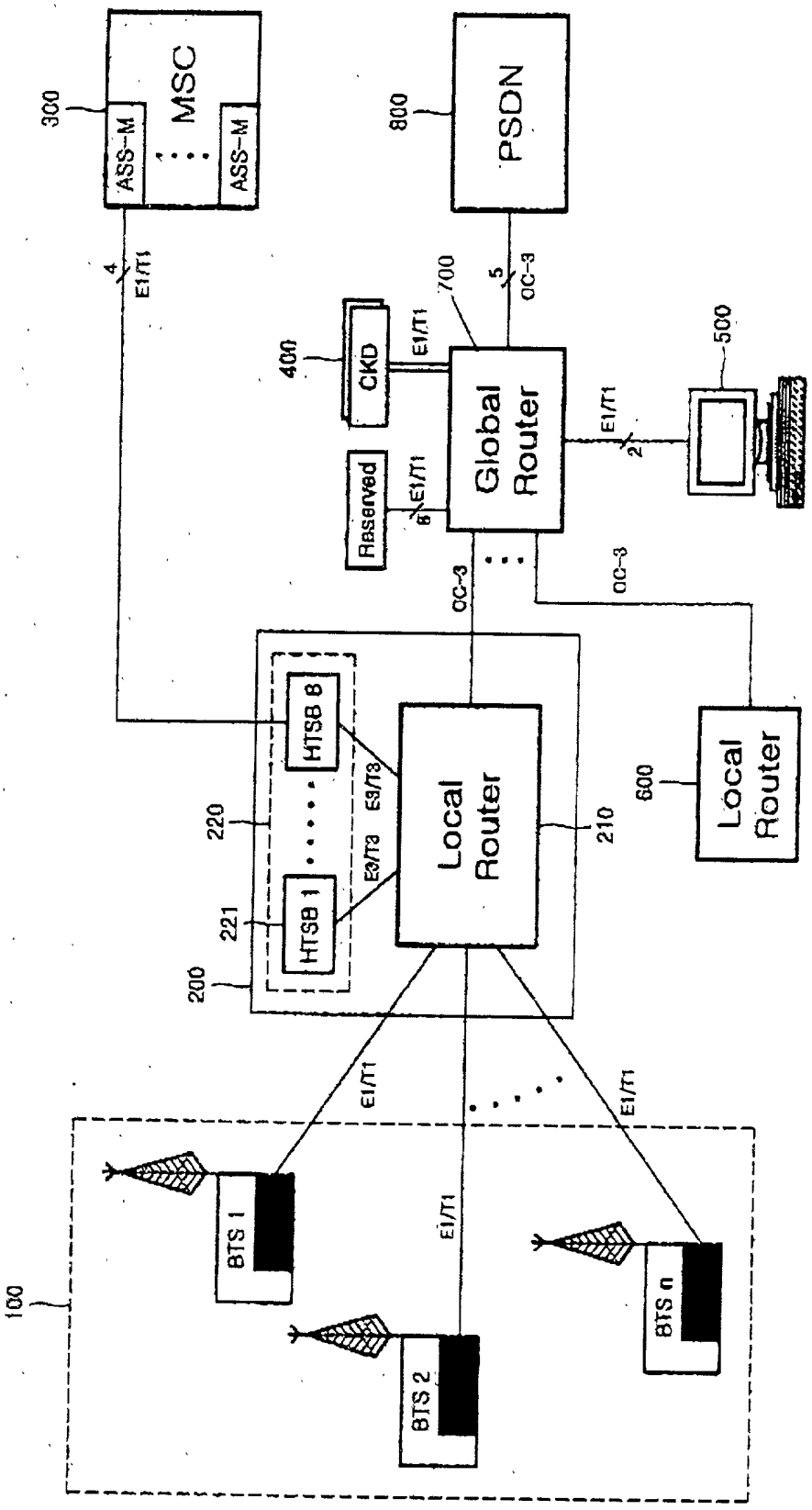

MSC
ASS-M
ASS-M
300
PSDN
800
4
E1/T1
5
OC-3
700
CKD
400
E1/T1
Global Router
500
Reserved
8
E1/T1
2
E1/T1
OC-3
OC-3
HTSB 8
HTSB 1
220
221
E3/T3
E3/T3
Local Router
210
600
Local Router
200
E1/T1
E1/T1
E1/T1
BTS 1
BTS 2
BTS n
100

FIG. 2

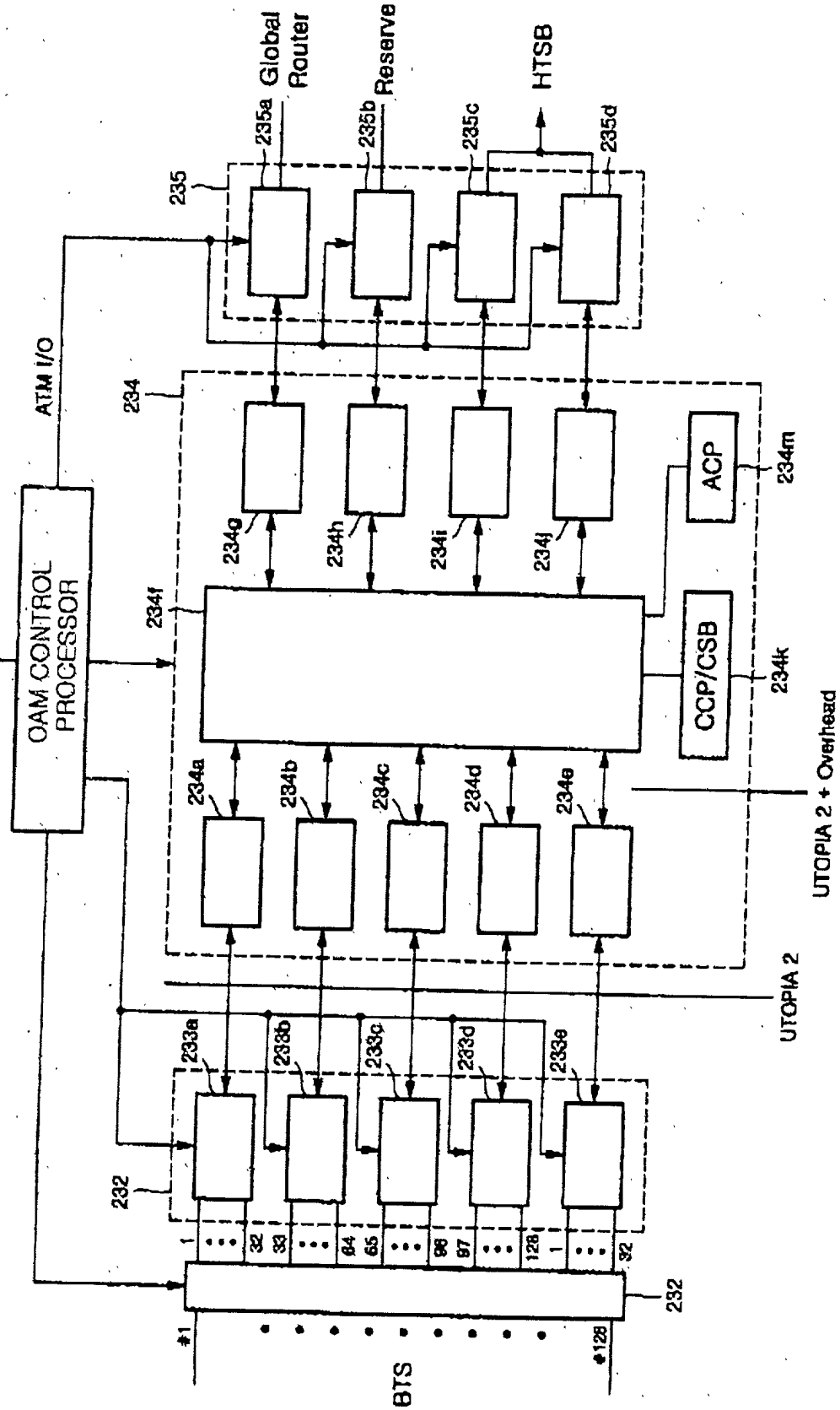
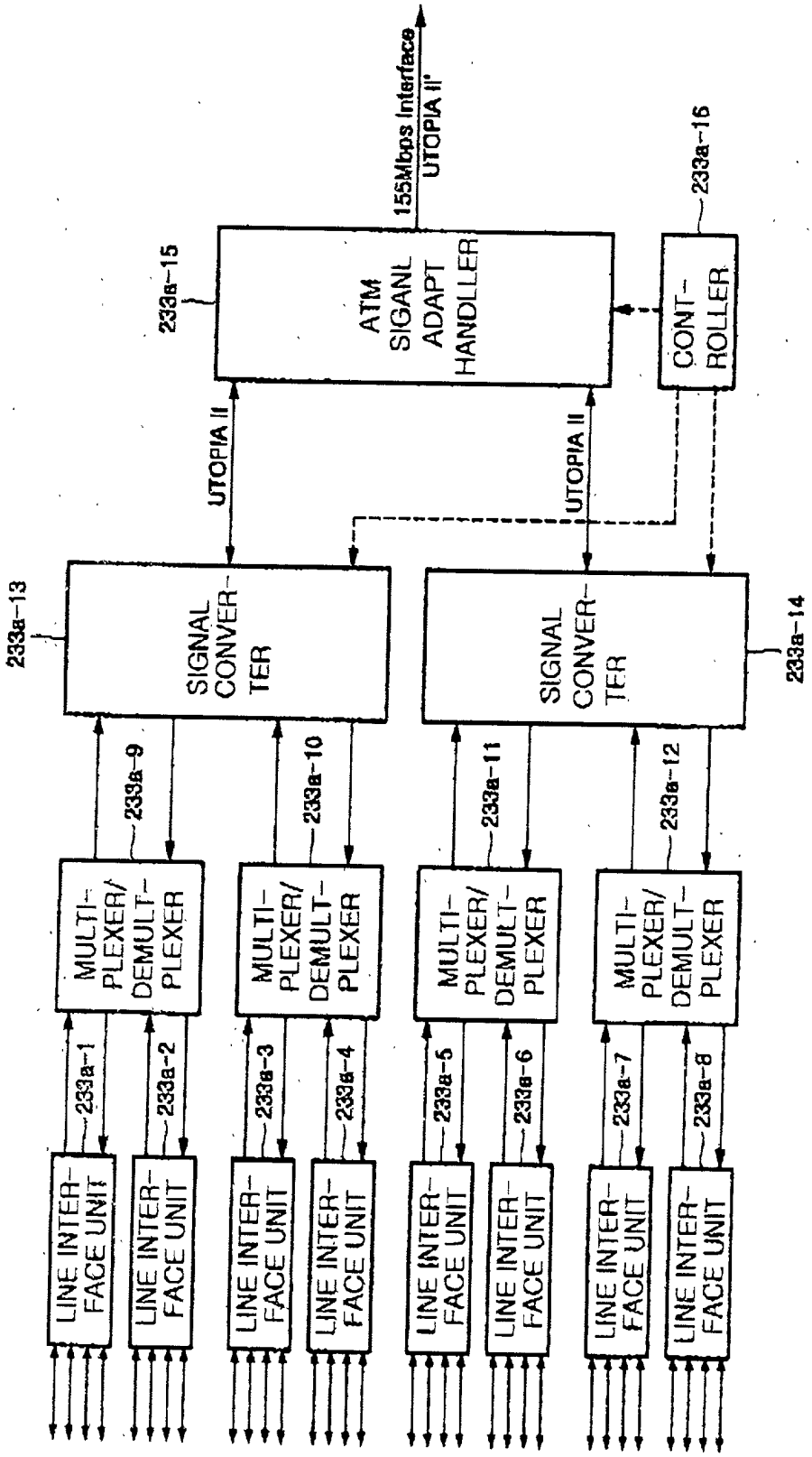

Global Router
Reserve
HTSB
235a
235b
235c
235d
235
ATM I/O
234
234g
234h
234i
234j
ACP
234m
OAM CONTROL PROCESSOR
231
234f
CCP/CSB
234k
234a
234b
234c
234d
234e
UTOPIA 2 + Overhead
UTOPIA 2
233a
233b
233c
233d
233e
232
1
32
33
64
65
96
97
128
1
32
232
#1
#128
BTS

FIG. 3

FIG. 4


155Mbps Interface
UTOPIA II'
233a-15
ATM SIGANL ADAPT HANDLLER
233a-16
CONT-ROLLER
UTOPIA II
UTOPIA II
233a-13
SIGNAL CONVER-TER
SIGNAL CONVER-TER
233a-14
233a-9
233a-10
233a-11
233a-12
MULTI-PLEXER/ DEMULT-PLEXER
MULTI-PLEXER/ DEMULT-PLEXER
MULTI-PLEXER/ DEMULT-PLEXER
MULTI-PLEXER/ DEMULT-PLEXER
233a-1
233a-2
233a-3
233a-4
233a-5
233a-6
233a-7
233a-8
LINE INTER-FACE UNIT
LINE INTER-FACE UNIT
LINE INTER-FACE UNIT
LINE INTER-FACE UNIT
LINE INTER-FACE UNIT
LINE INTER-FACE UNIT
LINE INTER-FACE UNIT
LINE INTER-FACE UNIT

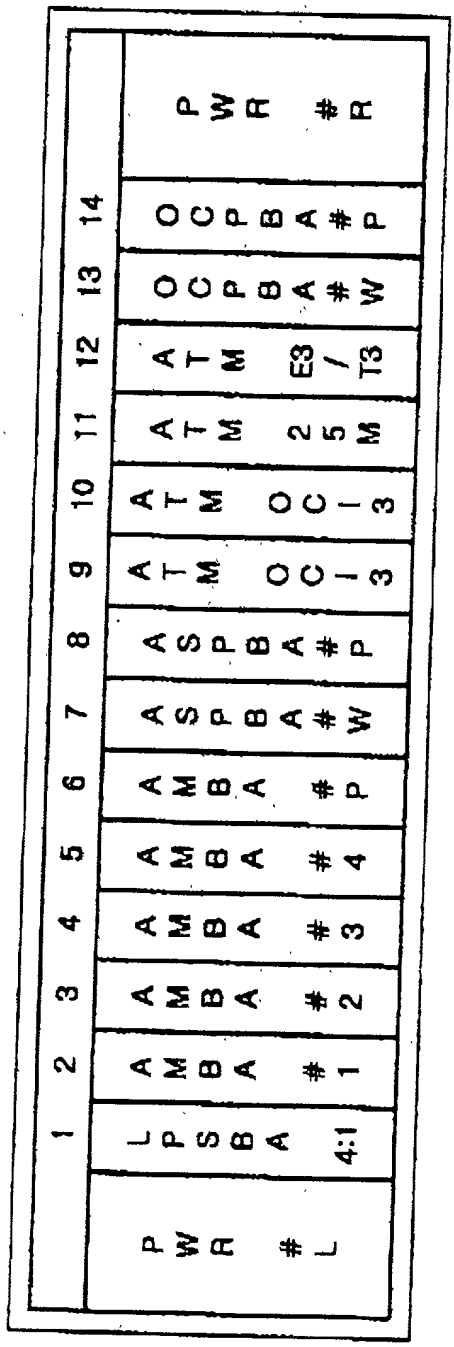
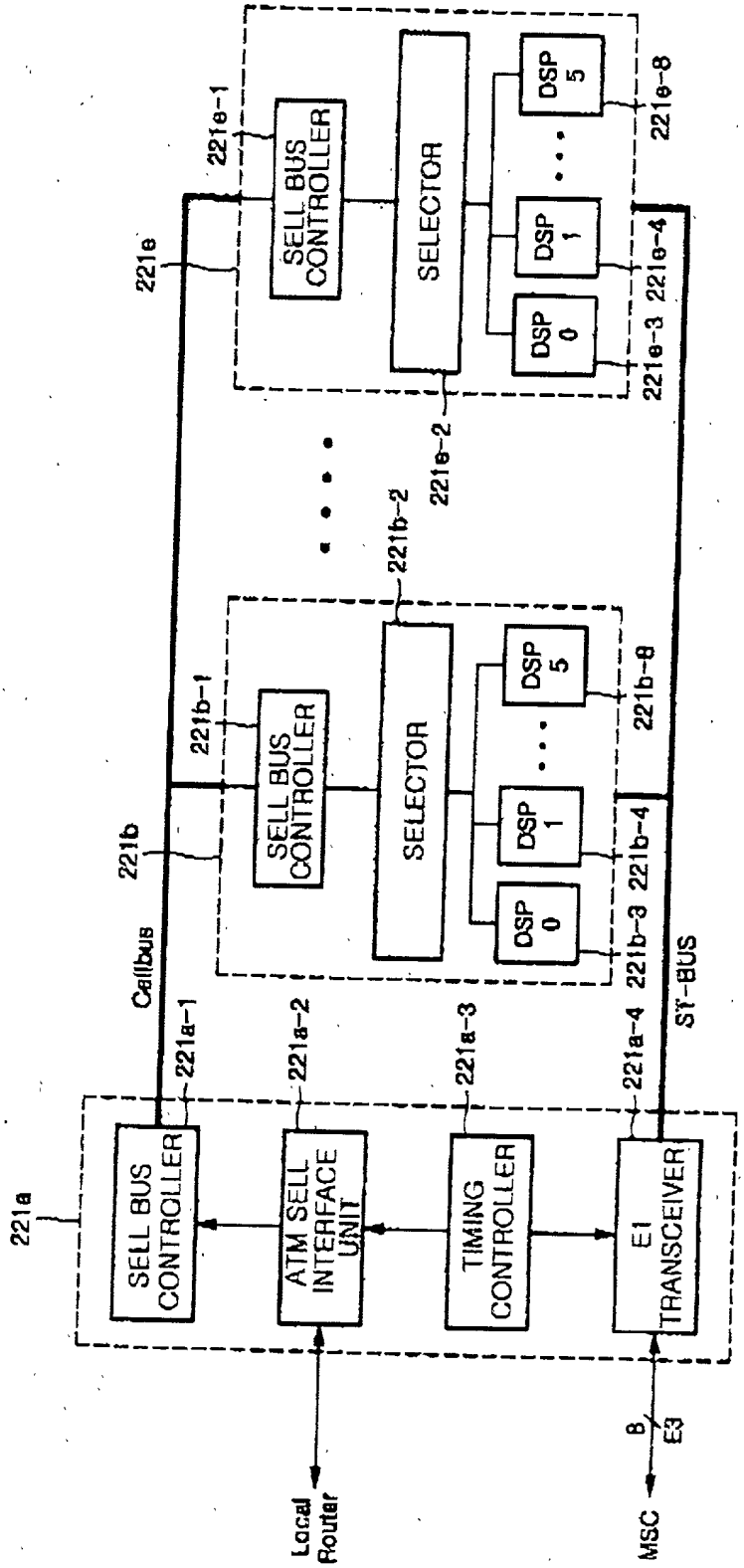

1 2 3 4 5 6 7 8 9 10 11 12 13 14
PWR #L
LPSBA 4:1
AMBA #1
AMBA #2
AMBA #3
AMBA #4
AMBA #P
ASPBA #W
ASPBA #P
ATM OC-3
ATM OC-3
ATM 25M
ATM E3/T3
OCPBA #W
OCPBA #P
PWR #R

FIG. 5

FIG. 6


221a
SELL BUS CONTROLLER
ATM SELL INTERFACE UNIT
TIMING CONTROLLER
E1 TRANSCEIVER
221a-1
221a-2
221a-3
221a-4
Callbus
ST-BUS
221b
221b-1
221b-2
221b-3
221b-4
221b-8
221e
221e-1
221e-2
221e-3
221e-4
221e-8
SELECTOR
DSP 0
DSP 1
DSP 5
Local Router
MSC
8
E3

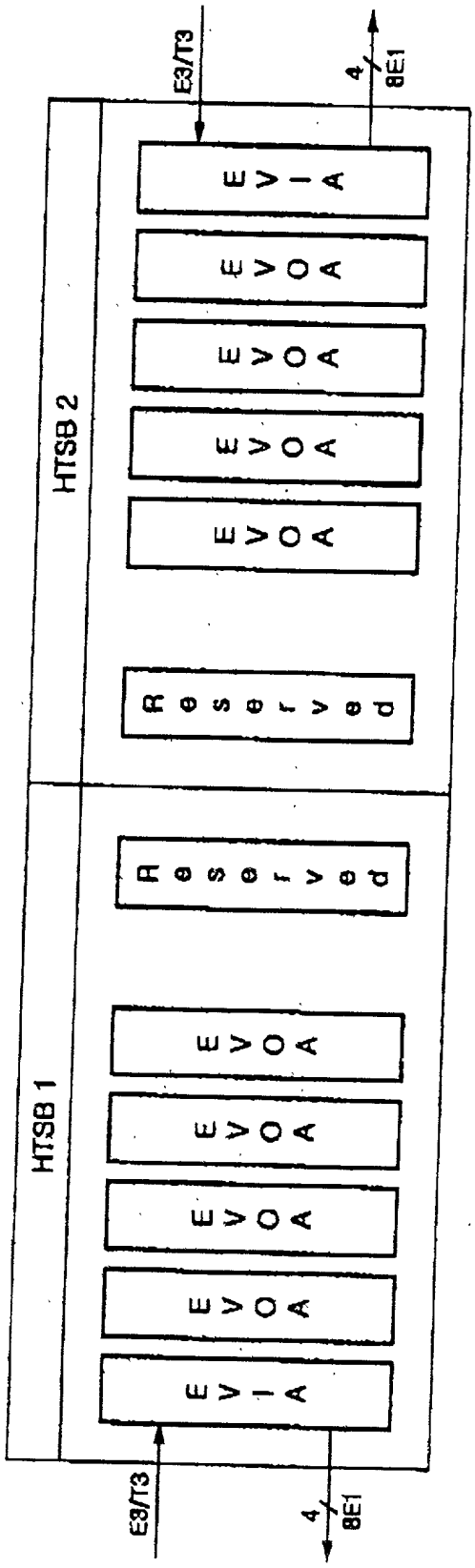

E3/T3
4/8E1
HTSB 2
E V - A
E V O A
E V O A
E V O A
E V O A
R e s e r v e d
R e s e r v e d
HTSB 1
E V O A
E V O A
E V O A
E V O A
E V - A
E3/T3
4/8E1

FIG. 7

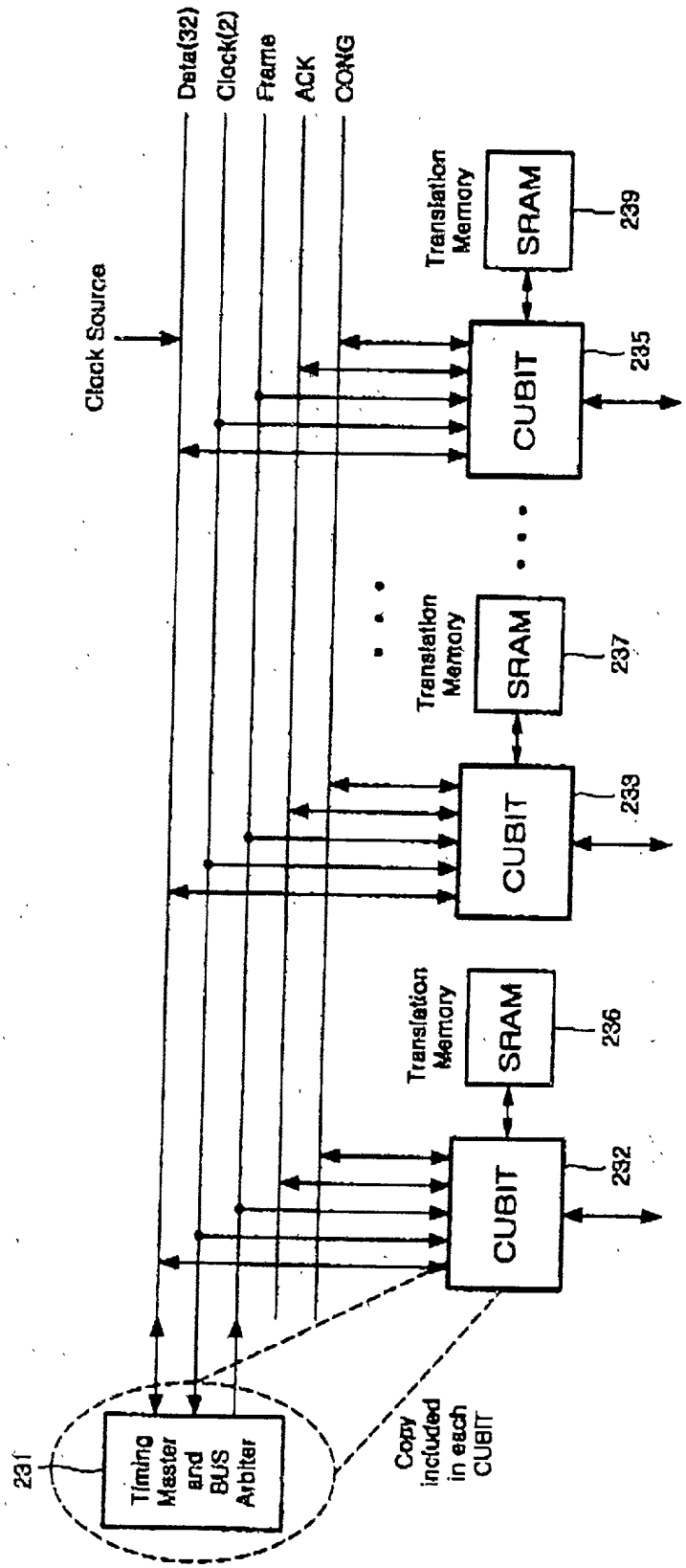

Data(32)
Clock(2)
Frame
ACK
CONG
Clock Source
Translation Memory
SRAM
239
CUBIT
235
Translation Memory
SRAM
237
CUBIT
233
Translation Memory
SRAM
236
CUBIT
232
231
Timing Master and BUS Arbiter
Copy included in each CUBIT

FIG. 8

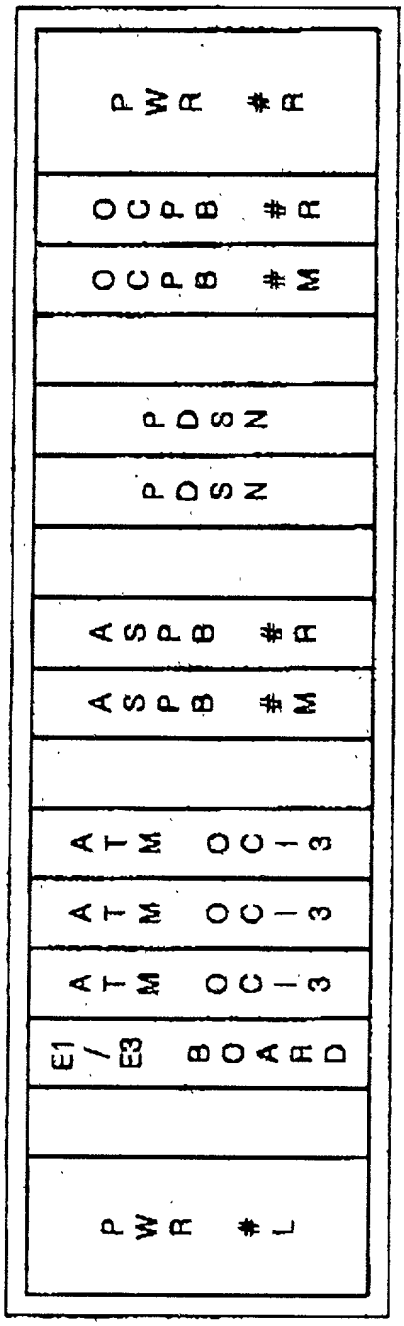

PWR #R
OCPB #R
OCPB #M
PDSN
PDSN
ASPB #R
ASPB #M
ATM OC-3
ATM OC-3
ATM OC-3
E1/E3 BOARD
PWR #L

FIG. 9